

INFORMATION DISCLOSURE CITATION PTO-1449	Atty. Docket No. 050637	Serial No. 10/551,391
Applicant(s): SASAO, Tsutomu, et al.		
	Filing Date: September 29, 2005	Group Art Unit: Not yet assigned

U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
_____	AA AB	Re. 34,363	R. H. Freeman	08/31/1993		

FOREIGN PATENT DOCUMENTS

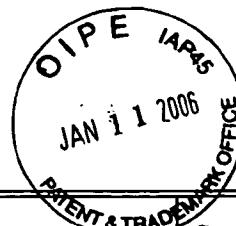
Document No.	Date	Country	Translation (Yes or No)
_____	AC AD		

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_____	AE	T. Sasao et al., "A Cascade Realization of Multiple-Output Function and Its Application to Reconfigurable Hardware," The Institute of Electronics, Information and Communication Engineers, Vol. 101, No. 3, Mie University, FTS2001-8, April 2001, pp. 57-64. English abstract is included. Discussed in the specification.
_____	AF	T. Sasao et al. "A Cascade Realization of Multiple-Output Function for Reconfigurable Hardware" International Workshop on Logic and Synthesis (IWLS01), Lake Tahoe, CA, June 12-15, 2001, pp. 225-230 w/cover page and the TOC, Discussed in the specification.
_____	AG	A. Tomita et al., " A Design of LUT-Array-Based PLD," The Institute of Electronics, Information and Communication Engineers, Vol. 100, No. 475, November 2000, pp. 173-178. English abstract is included.

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.T./



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_____	BG	M. Matsuura et al., "Compact Representations of BDDs for Multiple-Output Functions and Their Optimization," The Institute of Electronics, Information and Communication Engineers, Kitakyushu, VLS2001-100, November 2001, 6 sheets, English abstract is included.

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